Shayan Srinivasa Garani
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Research Interests

Broad area of mathematical systems science and complex systems engineering, applications of signal processing, information theory and coding towards physical nano memories, emerging areas in quantum information processing, mathematical biology and VLSI system architectures.

Education

Georgia Institute of Technology, Atlanta, GA **2002-2006**
Ph.D in Electrical and Computer Engineering. Minor in Mathematics.
Graduation date: July 2006
Dissertation Advisor : Prof. Steven W. McLaughlin
Dissertation Topic : Constrained Coding and Signal Processing for Holography.

University of Florida, Gainesville, FL **Aug. 1999 - May 2001**
M.S in Electrical and Computer Engineering.
Thesis Advisor : Prof. Jose C. Principe
Thesis Topic : An activity Diffusion Enhancement to Vector Quantizers.

University of Mysore, (S.J.C.E., Mysuru) India **Aug. 1993 - Aug. 1997**
B.E in Electronics and Communication Engineering, University rank holder.
Project Thesis Advisor : Prof. Ashok Rao
Project Thesis Topic : Speech and Image Compression through Wavelets.

Employment History

Indian Institute of Science, Bengaluru, India **June 2018 - present**
Title: Associate Professor, Department of Electronic Systems Engineering
Director : Physical Nano-memories, Signal and Information Processing Systems Laboratory

Indian Institute of Science, Bengaluru, India **July 2012 - June 2018**
Title: Assistant Professor, Department of Electronic Systems Engineering
Director: Physical Nano-memories, Signal and Information Processing Systems Laboratory

Western Digital, Irvine, California, U.S.A **Fall 2012 - 2013**
Title: Technology Consultant

Western Digital, Irvine, California, U.S.A **2010 - 2012**
Title: Sr. Principal Staff Engineer/Sr. Engineering Manager: Advanced Channels
Group: Advanced Technology Division under the office of the CTO.
Profile/Work Duties:

- Invent novel channel coding and signal processing schemes for recording systems, perform theoretical analysis for predicting the reliability of media recording channels and systems.
- Lead new initiatives for technological research and development towards high capacity and reliable storage systems. Establish a road map for future research activities.
- Interfacing with various engineering divisions to realize in-house R&D.

- Directing and managing funded research collaborations with universities.
- Chairman for IDEMA-ASTC signal processing. Developed signal processing roadmap for storage technology, solicited and reviewed university proposals along with other committee members. Established a framework for managing ASTC collaborations.
- Knowledge creation and dissemination through seminars, invited talks, publications and patents.
- Early promotion.

STMicroelectronics Inc., San Diego, California, U.S.A **2006 - 2010**
Title: Senior Innovative Systems Architect/Sr. Staff Member
Group: Read Channels Research and Development.
Profile/Work Duties:

- Invent error-correcting codes, constrained codes, develop signal processing algorithms for detection and noise prediction, perform theoretical analysis for predicting the reliability of error-correcting codes on media recording channels.
- Support design and verification teams to handoff architectures through software modules and documentation.
- Write white papers for the customer.
- Establish research and development leadership for two-dimensional magnetic recording (TDMR) and solid state memories. Architect algorithms that are efficient from performance/area/power and speed perspectives that went into actual Silicon. Actively involved in research proposals, patents and publications.
- Knowledge dissemination through teaching activities, seminars, invited talks and group discussions.
- Early promotion.

Western Digital, Lake Forest, California, U.S.A **Summer 2005**
Title: Summer Intern
Group: Advanced Channels Division.
Work Duties: Developed algorithms for post-ECC modeling of magnetic recording channels using hidden Markov models to analyze sector failure rates. The prediction model was theoretically solid and showed good correlation with real data from hard drives.

Broadcom Corporation, Bengaluru, India **June 2001 - Dec. 2001**
Title: Senior Design Engineer
Group: Digital Video Engineering.
Work Duties:

- Developed efficient algorithms for real time decoding of General Instruments' HITS streams for Personal Video Recording (PVR) feature that was put to actual Silicon on Broadcom chips.
- Software and debugging support for algorithm handoff.

Infosys Technologies Ltd, Bangalore, India **1997 - 1999**
Title: Software Design Engineer
Group: Nortel Networks - DMS 100 Switches and Spectrum
Work: Switching communications software for NORTEL DMS-100 switches and line timing synchronization for spectrum peripheral module.

Honors, Awards and Professional Distinctions

- Senior Member, OSA, 2016
- Western Digital master inventor award - 2012.
- Marquis who's who in science and technology - 2011.
- Senior Member, IEEE, 2011.
- Several patent awards and performance incentives at STMicroelectronics 2006-2010 (7 patents filed).
- Infosys-Nortel project of the year award - 1999.
- Best student paper award from the Institute of Electronics and Telecommunication Engineers, India, 1997.
- Awarded by the University of Mysuru and S. J. College of Engineering for securing 5^{th} rank for the Mysore University in Electronics and Communication Engineering stream - 1997.
- National Talent Search Scholar - 1991. Awarded by National Council of Educational Research and Training - Government of India. Ranked 8^{th} at the Karnataka state level.
- Awarded by the Chief Minister and the Minister of State for Education for securing 15^{th} rank for the state out of nearly 500,000 - State Government of Karnataka, India - 1991. Several other prizes from Bangalore teachers' association and the Rotary Club among many others for securing state rank.
- Best boy award (out of nearly 1000 students), Vijaya High School, Bengaluru 1991. Several academic achievement prizes during high school and pre-high school days.

Professional Activities: Editor/Technical Paper Reviews

- Editor, IETE Review Journal, Taylor and Francis Publishers (2014-present).
- Lead Guest Editor for IEEE JSAC 2016.
- Reviewer for IEEE Transactions on Communications, Signal Processing, Information Theory, Magnetics, Communication Letters, JSAC, Circuits and Systems-I and II, Acoust. Speech. and Language Proc., Neural Networks and Learning Systems, VLSI.
- Reviewer for Optical Engineering, Journal for Electronic Imaging - SPIE.
- Reviewer for EURASIP - Journal of Applied Signal Processing.
- Reviewer for Journal on Real Time Imaging - Springer-Verlag.
- Technical program committee member: IEEE international conferences: Globecom 2012-2017 (Quantum and Data Storage tracks), ICC 2013-2017, ICNC 2013, ICCVE 2012-2014, CONECCT 2013-2014, SPCOM 2014 (Publications chair).
- Organizing committee for summer Music school (Muster) at IISc, May. 2016.
- IEEE ICC 2018 Data Storage Track Chair.

Professional Activities: Research Grant Reviews

- Reviewer for American Mathematical Society research proposals.
- Reviewer for IDEMA-ASTC signal processing proposals.

- Reviewer for proposals within Dept. of Science and Technology.
- Reviewer for startup proposals for Govt. of India/Karnataka through Indian Knowledge Park.
- Reviewer for FONDECYT- Chile Science Foundation research proposals.

Professional Activities: Chair/Leadership initiatives

- Chairman, IEEE Data Storage Technical Committee (2019-2020).
- Chairman, Photonic Detection, Member, Optical society of America (2014-2017).
- Chairman, IEEE Data Storage Technical Committee (Awards Committee, 2015).
- Vice Chairman, Academics, IEEE Data Storage Technical Committee, 2016.
- Technology committee chairman for signal processing and channels research within advanced storage technology consortium (ASTC) under international disk drive equipment and materials association (IDEMA) (2011-2012). Western digital representative as a member of the technology committee (2012). Co-chair for the overall technological committee (2012).
- Senior Member, IEEE Communications, Information Theory and Magnetics Societies.
- Senior Member, Optical Society of America.

Professional Activities: Startups

- Advisor, clytics Inc.
- Co-founder, Compmusica.

Professional Activities: Academic Services

- Committee member for EECS webpage, 2018-present.
- Member of the senate committee for NPTEL, 2018-present.
- Chair of the Electrical Sciences division recommendations committee towards identifying academic and administrative policies for national and international accreditation, 2016.
- Faculty fellow from Indian National Academy of Sciences for recruiting and mentoring talented under graduate students across the country as part of internships.
- Faculty co-ordinator for M.Tech 2013-2015 within ESE department at IISc.
- Invited examiner for thesis defense within IISc, and in various universities at the national level.
- Invited for expert guidance into undergraduate syllabus structuring for Electronics and Communication Engg. at NITK Suratkal.
- Part of the team for conducting GATE and KVPY Indian national level exams.

Post-Doctoral Researchers

- Dr. Yiming Chen (Western Digital Corporation) (Summer 2011). Current position as principal engineer within Western Digital advanced channels division, U.S.A.

Doctoral Students

- Zitha Sasindran: *"Music signal processing,"* (Ph.D, ESE department, IISc) (Joined Fall 2017, ongoing)
- Arijit Mondal: *"VLSI architectures for codes and applications to memories,"* (Ph.D, ESE department, IISc) (Joined Fall 2015, ongoing)
- Priya Nadkarni: *"Quantum error correcting codes,"* (Ph.D, ESE department, IISc) (Joined Fall 2015, ongoing)
- Amrutha Machireddy: *"Convolution neural networks and temporal coding,"* (Ph.D, ESE department, IISc) (Joined Fall 2015, ongoing)
- Shounak Roy: *"Two-dimensional algebraic error correction codes,"* (Ph.D, ESE department, IISc) (Joined Fall 2013, ongoing)
- Ankur Raina: *"Information theory and coding for quantum secure channels,"* (Ph.D, ESE department, IISc) (Joined Fall 2013, ongoing)
- Prayag Gowgi: *"Spatio-temporal Memories: Theory and Algorithms,"* (Ph.D, ESE department, IISc) (Graduated in Jan. 2019)
- Chaitanya Kumar Matcha: *"Signal processing and Coding for Two-Dimensional Magnetic Recording,"* (Ph.D, ESE department, IISc) (Graduated in July 2018)

Masters Students

- A. Sreelakshmi *"Design architecture of an embedded zero-tree wavelet decoder,"* (M. Tech, ESE department, IISc) (In progress)
- Nimisha Jose and G. Aravindhan *"NAND channel modeling and ECC Techniques,"* (M. Tech, ESE department, IISc) (In progress)
- Sebin Jose *"Asynchronous implementation of the Viterbi detector,"* (M.E Microelectronics, ESE department, IISc) (Graduated summer 2017, Digital Design Engineer at Juniper Networks)
- Anil George *"Algorithms and design architecture for timing recovery in data storage channels,"* (M.E Microelectronics, ESE department, IISc) (Graduated summer 2017, Scientist with Indian Space Research Org.)
- Arnab Dey *"Asynchronous circuits for hard and soft decision Viterbi detectors,"* (M.E Microelectronics, ESE department, IISc) (Graduated summer 2016, Soc Designer at Intel Corporation)
- Suresh Alasatri and Palthiya Maanu *"Base ṣadja, meḷakarta rāga identification, modeling and synthesis of gamakas,"* (M.Tech, ESE department, IISc) (Graduated summer 2016, Pursuing Ph.D at City University of Hong Kong, Junior executive at Airports Authority of India)
- Vamshikrishna Yalamaddi and Thatimattala S. V. Satyannarayana *"Design architecture and implementation of a high throughput low latency Reed-Solomon decoder,"* (M.Tech, ESE department, IISc) (Graduated summer 2016, Digital design engineer at Nvidia Corporation and Scientist at Indian Space Research Org. respectively)

- Saugata Datta *"Design architecture of a non-uniformly quantized low latency one and two-dimensional soft output Viterbi detectors,"* (M.E Microelectronics, ECE department, IISc) (Graduated summer 2015, Analog design engineer at Texas Instruments, Bangalore)
- Nithin Raveendran: *"A modified sum-product algorithm over graphs with short cycles,"* (M.Sc, ESE department, IISc) (Fall 2012 - Summer 2015, Pursuing Ph.D at University of Arizona Prof. Vasić group.)
- Brijesh P. Reddy: *"Two-dimensional timing recovery using phase-locked loops,"* (M.Tech, ESE department, IISc) (Graduated summer 2014, Processor design engineer at Applied Microcircuits Corporation, Bangalore)
- Arijit Mondal *"Design of a min-sum LDPC decoder for error correction,"* (M.E Microelectronics, ESE department, IISc) (Graduated summer 2014, PhD at IISc within PNSIL)

Undergraduate Interns/project assistants

- Harshitha Srinivas: Fall 2015-Sep. 2018 (Project Assistant, PNSIL, Secretarial Services)
- Arathy Nair: Fall 2017 (Implementation of signal generators on FPGA)
- Varuni Rao: Spring 2016-Aug. 2016 (Project Assistant, Code implementation and music analysis)
- Tarun Khandelwal: Fall 2015-2017 (Project Assistant, Detector implementation)
- Eeshan Modak: Spring 2014-2016 (Worked on timing recovery methods, Currently at Celerix Tech)
- Praveen Kumar: Fall 2012-2015 (Worked on building a music automaton, Currently software engineer at Cisco Inc.)
- Many undergrad students recruited via Indian academy of sciences that spent summers within the lab since 2013.

Funded Research/Grant Awards

- **Chief-PI: Nand modeling and ECC**
  Funding Source: Toshiba Corp., 20 Lakhs, (2017-2019),
- **Chief-PI: Indo US Collaborations: Data Storage Research**
  Funding Source: Dept. of Science and Technology (India) and Dept. of State (USA), 50 Lakhs, (2016-2018),
- **Co-PI: Energy Analytics - Startup Initiative.**
  Funding Source: Shakti Foundation, 50 Lakhs, (2015-2016),
- **Chief-PI: Modeling, signal processing and coding for two-dimensional magnetic recording.**
  Funding Source: Department of Electronics and Information Technology, 50 Lakhs ($100K), (2014-2017),
- **Chief-PI: Timing recovery techniques and architectures for two-dimensional data storage channels.**
  Funding Source: Department of Science and technology, 37 Lakhs, ($74K) (2013-2016),
- **Chief-PI: Classical and quantum LDPC codes: Constructions and bounds**
  Funding Source: IISc Space Technology Cell, 20 Lakhs, ($40K) (2012-2015),
- **Chief-PI: Start up grant**
  Funding Source: IISc, 34 Lakhs, ($74K) (2012-2013),

- **Co-PI: LDPC codes with guaranteed error performance**
  Funding Source: U. C. Discovery Grant, $\$15,000$, (2011-2012),

Books/Monographs

1. **Constrained coding and signal processing for holography**, Author: Shayan Garani Srinivasa, *VDM-Verlag*, ISBN-10: 3836467054, Germany, Aug. 2008.

Book Chapters

1. **Data dependent adaptive prediction and classification of video sequences**Authors: A. Machireddy and S. S. Garani, Editors: Rutkowski et al. *Springer-Verlag: Lecture notes in Comp. Sc.*, ISBN: 978-3-319-91253-0, Proc. 17^{th} Intl . Conf. on Art. Intell. and Soft. Comput., Zakopane, June 2018.
2. **Dynamic vector quantization of speech, Title: Advances in self-organizing maps**, Authors: S. Garani and J. C. Principe, Editors: Nigel Allinson, Hujun Yin, Lesley Allinson and Jon Slack, *Springer-Verlag: Lecture notes in Comp. Sc.*, ISBN-10: 1852335114, Proc. WSOM, London, July 2001.

Journal Special Issues: Edited Issues

1. "Channel Modeling, Coding and Signal Processing for Novel Physical Memory Devices and Systems," **Lead Editor** along with Tong Zhang, Ravi Motwani, Haralampos Pozidis and Bane Vasić, *IEEE. Jour. Select. Areas in Comm.*, Sep. 2016.

Journal Publications

1. S. S. Garani and H. Seshadri "An algorithmic approach to South Indian classical music," accepted to *Jour. Music and Mathematics*, Dec. 2018.
2. S. Roy, A. Mondal and S. S. Garani, "A fast and efficient two-dimensional Chien search algorithm and design architecture," in *IEEE. Comm. Lett.,* Jan. 2019.
3. P. Gowgi and S. S. Garani, "Temporal self-organization: A reaction-diffusion framework for spatio-temporal memories," Early access *IEEE. Trans. Neural Nets. and Learning Sys.,* July 2018.
4. S. S. Garani, L. Dolecek, J. R. Barry, F. Sala and B. Vasić, "Signal processing and coding for two-dimensional magnetic recording: An overview," *Proc. of the IEEE,* Feb. 2018.
5. A. Mondal, T. Satyannarayana, V. K. Yalamaddi and S. S. Garani, "Efficient coding architectures for Reed Solomon and low density parity check decoders for magnetic and other data storage systems," *IEEE. Trans. Magn.,* Feb. 2018.
6. C. K. Matcha, S. Roy, M. Bahrami, B. Vasić and S. G. Srinivasa, "2D LDPC codes and joint detection and decoding for two-dimensional magnetic recording," *IEEE. Trans. Magn.,* Feb. 2018.
7. C. K. Matcha and S. G. Srinivasa, "Joint timing recovery and signal detection for two-dimensional magnetic recording," *IEEE. Trans. Magn.*, Feb. 2017.
8. C. K. Matcha and S. G. Srinivasa, "Defect detection and burst erasure correction for TDMR," *IEEE. Trans. Magn.*, Nov. 2016.

9. S. Datta and S. G. Srinivasa, "Design architecture of a two-dimensional separable iterative soft output Viterbi detector," *IEEE. Trans. Magn.*, Jan. 2016.

10. M. Bahrami, C. K. Matcha, S. Roy, S. G. Srinivasa and B. Vasić, "Investigation into harmful patterns over multi-track shingled magnetic detection using the Voronoi model," *IEEE. Trans. Magn.*, Dec. 2015.

11. C. K. Matcha and S. G. Srinivasa, "Generalized partial response equalization and data dependent noise predictive signal detection over media models for TDMR," *IEEE. Trans. Magn.*, Oct. 2015.

12. B. P. Reddy, S. G. Srinivasa and S. Dahandeh, "Timing recovery algorithms and architectures for two-dimensional magnetic recording systems," *IEEE. Trans. Magn.*, Apr. 2015.

13. S. G. Srinivasa, Y. Chen and S. Dahandeh, "A communication-theoretic framework for TDMR channel modeling: Performance evaluation of coding and signal processing methods," *IEEE. Trans. Magn.*, Mar. 2014.

14. Y. Chen and S. G. Srinivasa, "Joint self-iterating equalization and detection for two-dimensional intersymbol-interference channels," *IEEE. Trans. Comm.*, vol. 61, no. 8, pp. 3219-3230, Aug. 2013. (**Nominated for the best paper award**)

15. S. G. Srinivasa, "Holographic imaging: Information recording and retrieval," *Jour. Ind. Inst. Sci.*, vol. 93, no. 1, pp. 35-46, Mar. 2013. (Invited review article)

16. S. G. Srinivasa, O. Momtahan, A. Karbaschi, S. W. McLaughlin, F. Fekri and A. Adibi, "Volumetric storage limits and space volume multiplexing trade-offs for holographic channels," *SPIE. Journal of Opt. Engineering*, vol. 49, no. 1, Jan. 2010.

17. S. G. Srinivasa and A. Weathers, "An efficient on-the-fly encoding algorithm for binary and finite-field LDPC codes," *IEEE. Comm. Lett.*, vol. 13, no. 11, pp. 853-855, Nov. 2009.

18. S. G. Srinivasa and S. W. McLaughlin, "Capacity bounds for two-dimensional asymmetric M-ary $(0, k)$ and (d, ∞) runlength-limited channels," *IEEE. Trans. Comm.*, vol. 57, no. 6, pp. 1584-1587, June. 2009.

19. S. G. Srinivasa, P. Lee and S. W. McLaughlin, "Post-error correcting code modeling of burst channels using hidden Markov models with applications to magnetic recording channels," *IEEE Trans. Magn.*, vol. 43, no. 2, pp. 572-579, Feb. 2007.

20. J. C. Principe, N. R. Euliano and S. Garani, "Principles and networks for self organization in space time," Special Issue of Journal of Neural Networks, *Elsevier Press*, vol. 15, pp. 1069-1083, Oct. 2002.

Patents

1. Method and apparatus for joint adaptation of two-/multi-dimensional equalizer and partial response target, Inventors: Shayan Srinivasa Garani, Chaitanya Kumar Matcha, Arnab Dey, U.S. Patent No. 10,026,441, July. 2018.

2. Identifying a defect in a data-storage medium, U.S. Patent No. 9,324,370, with Sivagnanam Parthasarathy, April 2016.

3. Method and system for monitoring data channel to enable use of dynamically adjustable LDPC coding parameters in a data storage system, U.S. Patent No. 9,214,963, with Kent D. Anderson, Anantha Raman Krishnan, Guangming Lu, Shafa Dahandeh, Andrew J. Tomlin, Dec. 2015.

4. Systems and methods for improved encoding of data in data storage devices, U.S. Patent No. 9,203,434, Sole inventor, Dec. 2015.

5. Decoding data stored in solid-state memory, U.S. Patent No. 8,990,668, with Anantha Raman Krishnan and Kent Anderson, Mar. 2015.

6. Data storage device tracking log-likelihood ratio for a decoder based on past performance, U.S. Patent No. 8,856,615, with Anantha Raman Krishnan, Kent Anderson and Shafa Dahandeh, Oct. 2014.
7. Methods and devices for joint two-dimensional self-iterating equalization and detection, U.S. Patent No. 8,760,782, with Yiming Chen, June 2014.
8. Constrained on-the-fly interleaver address generation, U.S. Patent No. 8,625,220, with Sivagnanam Parthasarathy and Sudha Thipparthi, Jan. 2014.
9. Methods and devices for two-dimensional iterative multi-track based MAP detection, U.S. Patent No. 8,582,223, with Yiming Chen, Nov. 2013.
10. Encoding apparatus, system and method using LDPC codes, U.S. Patent No. 8,397,125, Sole inventor, March. 2013.
11. Adaptive data dependent noise prediction, U.S. Patent No. 8,290,102, with Mustafa Kaynak, Stefano Valle and Sivagnanam Parthasarathy, 2012.
12. Interlaced iterative system design for 1K-byte block with 512 byte LDPC code words, U.S. Patent No. 8,255,768, with Xinde Hu, Sivagnanam Parthasarathy, Anthony Weathers and Richard Barndt, 2012.
13. Channel constrained code aware interleavers, U.S. Patent No. 8,055,973, with Nicholas Richardson and Xinde Hu, 2011.
14. Machine based music synthesis, Inventors: Shayan Srinivasa Garani, Harish Seshadri and Praveen Nandakumar, *Patent filed Indian PTO,* Dec. 2013.
15. Reed-Solomon decoders and decoding methods, Inventors: Shayan Srinivasa Garani, Thattimattala Satyannarayana, Vamshi Krishna Yalamaddi, *International Patents filed,* July 2017.
16. Method and apparatus for interpolative timing recovery for two-dimensional magnetic recording systems, Inventors: Shayan Srinivasa Garani, B. P. Reddy, E. Modak, *PCT filed,* Aug. 2018.

Conference Publications

1. P. Nadkarni and S. S. Garani, "Entanglement assisted quantum Reed-Solomon codes," in *IEEE. Info. Theory and Appl.,* San Diego, Feb. 2019.
2. P. Nadkarni and S. S. Garani, "Encoding of quantum stabilizer codes over qudits with $d = p^k$," in *IEEE. Globecom.,* Abu Dhabi, Dec. 2018.
3. C. K. Matcha and S. S. Garani, "2D linear detector based on generalized belief propagation algorithm," in *IEEE Proc. Fifty-sixth Allerton Conference on Computers, Control and Communications,* Urbana Champaign, U.S.A., Oct. 2018.
4. A. B. Nair, A. Mondal and S. S. Garani "A low-complexity hardware AWGN channel emulator on FPGA using central limit theorem," in *IEEE. 61st Intl. Midwest Symp. on Circuits and Syst.,* Windsor, Aug. 2018.
5. P. Gowgi, A. Machireddy and S. S. Garani, "Priority-based soft vector quantization feature maps," in *IEEE. Proc. Intl. Joint Conf. on Neural Netw.,* Rio Di Janeiro, July 2018.
6. S. Roy and S. S. Garani, "Two-dimensional algebraic error correcting codes," in *IEEE. Info. Theory and Appl.,* San Diego, Feb. 2018.
7. P. Nadkarni, A. Raina and S. G. Srinivasa, "Recovery of distributed quantum information from a node failure using graph states," in *IEEE. Globecom.,* Singapore, Dec. 2017.
8. P. Nadkarni and S. G. Srinivasa, "Entanglement assisted quantum binary tensor product codes," in *IEEE. Inform. Theory Work.,* Kaohsiung, Taiwan, Nov. 2017.

9. A. Raina, P. Nadkarni and S. G. Srinivasa, "Recovery of distributed quantum information in quantum networks," in *Frontiers in Opt.,* Washington DC, Sep. 2017.

10. C. K. Matcha, S. Roy, M. Bahrami, B. Vasić and S. G. Srinivasa, "2D LDPC codes and joint detection and decoding for two-dimensional magnetic recording," in *IEEE. Magn. Record. Conf.,* Tsukuba, Aug. 2017. (Invited Lecture, 2 pages)

11. A. Dey, S. Jose, K. Varghese and S. G. Srinivasa "A High-Throughput Clock-Less Architecture for Soft-Output Viterbi Detection," in *IEEE. 60th Intl. Midwest Symp. on Circuits and Syst.,* Boston, Aug. 2017.

12. T. Khandelwal, K. Rajwanshi, P. Bharadwaj, S. G. Srinivasa and R. Sundaresan "Exploiting appliance state constraints to improve appliance detection," in *ACM. e-Energy.,* Hongkong, May 2017.

13. N. Raveendran, P. J. Nadkarni, S. S. Garani and B. Vasić "Stochastic resonance decoding for quantum LDPC codes," in *IEEE. Intl. Conf. Comm.,* Paris, May 2017.

14. A. Raina and S. G. Srinivasa, "Multiparty quantum communication using hyper-entangled states," in *IEEE. Globecom.,* Washington DC, Dec. 2016.

15. C. K. Matcha and S. G. Srinivasa, "Joint timing recovery and signal detection for two-dimensional magnetic recording," in *IEEE. Magn. Record. Conf.,* Palo Alto, Aug. 2016. (Invited Lecture, 2 pages)

16. C. K. Matcha, M. Bahrami, S. Roy, S. G. Srinivasa and B. Vasić, "Generalized belief propagation based TDMR detector and decoder," in *IEEE. Intl. Symp. Inform. Theory,* Barcelona, July 2016.

17. P. Gowgi and S. Garani, "Density transformation and parameter estimation from back propagation algorithm," in *IEEE. Proc. Intl. Joint Conf. on Neural Netw.,* Killarney, July 2016.

18. E. Modak, B. P. Reddy and S. G. Srinivasa, "Optimum timing interpolation algorithm for 2-D magnetic recording systems," in *IEEE. Natl. Conf. Comm.,* Guwahati, India, Mar. 2016.

19. S. Datta, K. Varghese and S. G. Srinivasa, "A non-uniformly quantized high throughput soft output Viterbi detector on FPGA," in *IEEE Proc. VLSI,* Kolkata, India, Jan. 2016.

20. A. Raina and S. G. Srinivasa, "Entanglement and its role on the capacity of noisy two-Pauli channels," in *IEEE Proc. WRAP,* Bengaluru, India, Dec. 2015.

21. A. Raina and S. G. Srinivasa, "Eavesdropping on a quantum channel with a unitarily interacting probe," in *IEEE Proc. Globecom,* San Diego, U.S.A, Dec. 2015.

22. S. Roy and S. G. Srinivasa, "Two-dimensional error correcting codes using finite field Fourier transform," in *IEEE. Inform. Theory Workshop,* Jeju Island, Oct. 2015.

23. P. Gowgi and S. Garani, "Spatio-temporal map formation based on a potential function," in *IEEE. Proc. Intl. Joint Conf. on Neural Netw.,* Killarney, July 2015.

24. C. K. Matcha and S. G. Srinivasa, "A study on the implications of grain density distribution over the granular media model for TDMR," in *IEEE. Intermag.,* Beijing, Mar. 2015.

25. C. K. Matcha and S. G. Srinivasa, "Exact analysis of the performance of Viterbi detector for ISI Channels with quantized inputs," in *IEEE. Natl. Conf. Comm.,* Mumbai, Mar. 2015.

26. A. Raina and S. G. Srinivasa, "Quantum dense coding and teleportation using hyper entangled states," in *IEEE. Inform. Theory Appl. Workshop,* San Diego, Feb. 2015.

27. C. K. Matcha and S. G. Srinivasa, "Target design and low complexity signal detection for two dimensional magnetic recording," in *IEEE. Asia-Pacific Signal and Inform. Proc. Conf.,* Siem Reap, city of Angkor Wat, Cambodia, Dec. 2014.

28. C. K. Matcha, S. G. Srinivasa, S. M. Khatami and B. Vasić, "Two-dimensional noise-predictive maximum likelihood method for magnetic recording channels," in *IEEE. Intl. Symp. Inform. Theory and Appl.,* Melbourne, Oct. 2014.

29. A. Raina and S. G. Srinivasa, "Quantum communication over bit flip channels using entangled bipartite and tripartite states," in *IEEE Proc. Fifty-second Allerton Conference on Computers, Control and Communications,* Urbana Champaign, U.S.A, Oct. 2014.

30. B. P. Reddy, S. G. Srinivasa, and S. Dahandeh, "Timing recovery algorithms and architectures for two-dimensional magnetic recording systems," in *IEEE. Magn. Record. Conf.,* Berkeley, Aug. 2014.

31. B. P. Reddy and S. G. Srinivasa, "Two-dimensional signal processing for timing recovery using PLLs for storage channels," in *IEEE. China Summit and Intl. Conf. Signal and Inform. Processing,* Xi'an, July 2014.

32. N. Raveendran and S. G. Srinivasa, "A modified sum-product algorithm over graphs with isolated short cycles," in *IEEE. Proc. Intl. Symp. Inform. Theory,* Honolulu, July 2014.

33. N. Raveendran and S. G. Srinivasa, "An analysis into the loopy belief propagation algorithm for short cycles," in *IEEE. Proc. Intl. Conf. on Comm.,* Sydney, June 2014.

34. S. G. Srinivasa, "LDPC code designs based on $\sqrt{I}$ matrices," in *IEEE. Inform. Theory Appl. Workshop,* San Diego, Feb. 2014.

35. S. G. Srinivasa, Y. Chen and S. Dahandeh, "A communication-theoretic framework for TDMR channel modeling: Performance evaluation of coding and signal detection methods," in *IEEE. Magn. Record. Conf.,* Tokyo, Aug. 2013.

36. S. G. Srinivasa and H. Seshadri, "Music and symbolic dynamics: The science behind an art," in *IEEE. Inform. Theory Appl. Workshop,* San Diego, Feb. 2013.

37. Y. Chen and S. G. Srinivasa, "Performance-Complexity trade-offs of the 2-D iterative feedback signal detection algorithm," in *IEEE. Intl . Conf. Computing, Networking and Communications,* San Diego, Jan. 2013.

38. A. Amiri, S. G. Srinivasa, and L. Dolecek, "Quantization, absorbing regions and practical message passing decoders," in *IEEE. Proc. Asilomar Conference,* Monterey, Nov. 2012.

39. Y. Chen and S. G. Srinivasa, "Signal detection algorithms for two-dimensional intersymbol-interference channels," in *IEEE. Proc. Intl. Symp. Inform. Theory,* Cambridge, July 2012.

40. J. Zhang, J. Wang, S. G. Srinivasa, and L. Dolecek, "Achieving flexibility in LDPC code design by absorbing set elimination," in *IEEE. Proc. Asilomar Conference,* Monterey, Nov. 2011.

41. S. G. Srinivasa, O. Momtahan, A. Karbaschi, S. W. McLaughlin, A. Adibi, and F. Fekri, "M-ary, binary, and space-volume multiplexing trade-offs for holographic channels," in *IEEE. Proc. Globecom,* San Fransisco, Nov. 2006.

42. S. G. Srinivasa and S. W. McLaughlin, "Capacity lower bounds for two-dimensional M-ary (d, ∞) and $(0, k)$ runlength-limited channels," in *IEEE. Proc. Intl. Symp. Inform. Theory,* Seattle, pp. 1472-1476, July 2006.

43. S. G. Srinivasa, Patrick Lee, and S. W. McLaughlin, "Post-ECC modeling of magnetic recording channels using hidden Markov models," in *IEEE. Proc. Intl. Conf. on Comm.,* Istanbul, pp. 1249-1254, June 2006.

44. S. G. Srinivasa and S. W. McLaughlin, "Capacity bounds and coding Schemes for two-dimensional asymmetric k-constrained runlength-limited arrays," in *Proc. Forty-third Allerton Conference on Computers, Control and Communications., Illinois Univ. Press*, Monticello, IL-U.S.A., Oct. 2005.

45. S. G. Srinivasa and S. W. McLaughlin, "Signal recovery due to rotational pixel misalignment," in *IEEE. Proc. Intl. Conf. on Acoust., Speech and Signal Proc.,* pp. 121-124, Philadelphia, U.S.A., Mar. 2005.

46. S. G. Srinivasa and S. W. McLaughlin, "Enumeration algorithms for a class of (d_1,∞,d_2,∞) RLL arrays: Capacity estimates and coding schemes," in *IEEE. Proc. Inform. Theory Workshop,* pp. 141-146, San Antonio, U.S.A., Oct. 2004.

47. S. G. Srinivasa and S. W. McLaughlin, "Algorithms for constructing a class of (1,∞,d,k) codes and estimates for capacity," in *Proc. Forty-first Allerton Conference on Computers, Control and Communications., Illinois Univ. Press*, pp. 867-875, Monticello, IL-U.S.A., Oct. 2003.

48. S. Garani and J. C. Principe, "A spatio-temporal vector quantizer for missing samples reconstruction," in *IEEE. Proc. Intl. Joint Conf. on Neural Netw.,* vol. 4, pp. 2913-2917, June 2001.

Other National Level Conference Publications

1. S. G. Srinivasa and Josyer G. V, "An image coding and compression algorithm through PRQMF banks and wavelets," *IETE National Conference, Mysore*, 1997. (Awarded best student paper)

Manuscripts in Review

1. Several original articles on various topics in various stages of review.

Select Academic and Industrial Talks and Presentations (International Invited Speaking Engagements)

1. *'The role of academics, industry, government and international collaborations for skilled manpower development,'* The Indus Foundation, July 2017.
2. *'Two-dimensional equalization and detection,'* Department of Electrical and Computer Engineering, University of California, San Diego, May 2013. (*IEEE* sponsored)
3. *'Music and symbolic dynamics,'* Department of Electrical and Computer Engineering at the University of California, San Diego and University of Arizona, May 2013.
4. *'Information theory, signal processing and coding theory used in high-density optical recording,'* Link-a-media Devices, Santa Clara, June 2010.
5. *'Research trends in advanced data storage research,'* Department of Electrical Engineering, University of California, Irvine, Nov 2010.
6. *'Hidden Markov models in magnetic recording,'* Center for Magnetic Recording Research, San Diego, Oct. 2008.
7. *'Signal processing for holography,'* Broadcom Corporation, Longmont, Mar. 2006.
8. *'Post-ECC modeling,'* Western Digital, Lake Forest, California, Aug. 2005.

Select Academic and Industrial Talks (National level Invited Speaking Engagements outside IISc)

1. *'Curiosity driven research: An example where science meets arts,'*, Faculty Development Program, VVCE, Mysuru, Jan. 2019.

2. *'Interdisciplinary research: An example from data storage,'*, Faculty Development Program, VVCE, Mysuru, Jan. 2019.

3. *'Stochastic Processes and Applications,'*, MSRIT Faculty Development Program, Keynote Talk, Bengaluru, July 2017.

4. *'Computer Generated Music,'*, Special Invited Lecture at the 4th Intl. Music and Dance festival at Indiranagar Sangeetha Sabha, June 2017.

5. *'Multidimensional Data Storage: Channels Engineering,'*, Toshiba Corporation, Bengaluru, May 2017.

6. Invited by the All India Radio - Bengaluru for a narrative 2 hr. recording to an episode on 'Prapatti as envisaged by Saint Tyagaraja', Sep. 2016.

7. *'Music Signal Processing,'*, IEEE ICRAECT, Keynote Talk, Bengaluru, March 2017. Lecture at BMSIT on the same topic April 2017, Lecture at MSRIT Dec. 22 2017 on National Mathematics Day.

8. *'Coding for Communication Channels,'* Govt. Engg. College., NCCCSP, Wayanad, India, May 2016. (Plenary Talk)

9. *'Data centers and microservers,'* Samsung Data Storage Research Center, Bangalore, India, May 2014. (Industry invited lecture)

10. *'Music and symbolic dynamics: The science behind an art,'* CA Techologies, MSRIT Bangalore, India, May 2014, Sep. 2016. (Industry, academic invited lecture)

11. *'Mathematical techniques in signal processing and imaging,'* PSGTech, ECE dept, Coimbatore, India, Oct. 2013. (part of faculty quality improvement program)

12. *'Stochastic processes in engineering,'* RVCE, Mathematics dept, Bangalore, India, July. 2013. (part of faculty quality improvement program)

13. *'Linear algebra in biology,'* PESIT, Bangalore, ECE dept, India, July. 2013. (part of faculty quality improvement program)

14. *'Constrained coding and signal processing for holography',* Texas Instruments Bangalore, Oct. 2005.

15. *'Signal modeling and representation,'* Deepthi Electronics and Optics Ltd., Bangalore, India, Aug. 2003.

16. *'Multirate signal processing and sampling rate architectures,'* Broadcom Corporation, Bangalore, India, Dec. 2001.

Courses Offered/Taught

1. Basics of signal processing (New graduate level course), IISc- Bengaluru, Spring 2018.

2. Linear and non-linear programming - I (New graduate level course), IISc-CCE-Bengaluru, Spring 2018.

3. Neural networks and learning systems - I (New graduate level course introduced), IISc-Bengaluru, Spring 2017.

4. Selected topics in Markov chains and optimization (New graduate level course introduced with Prof. Joy Kuri), IISc-Bangalore, Fall 2014-2015.

5. Signal processing for data recording channels (New graduate level course introduced), IISc-Bangalore, Fall 2012. Taught during Fall 2012, Spring 2014, Spring 2016.

6. Mathematical methods and techniques in signal processing (New graduate level course introduced), IISc-Bangalore, Spring 2013, Fall 2014, Fall 2015, Fall 2016, Fall 2017, MOOC style Spring 2018, 2019.

7. Seminars and research lectures on advanced topics to industrial R&D members.

Miscellaneous

1. South-Indian classical vocalist sought after for concerts and lecdems by various organizations.
2. Advanced level Carnatic classical music teacher within the Indian community.

Academic References

Available upon request.